PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-003892

(43)Date of publication of application : 06.01.1999

(51)Int.Cl. H01L 21/3213
H01L 21/3065
H01L 21/3205

(21)Application number : 09-167909

(22)Date of filing : 11.06.1997

(71)Applicant : RICOH CO LTD

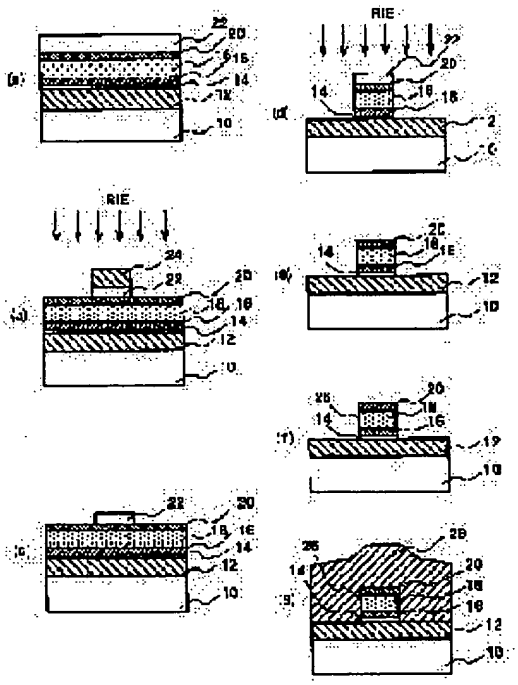
(72)Inventor : SATO SHINJI

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a copper wiring of low resistance and high reliability by preventing surface oxidation of the copper wiring etc., and easily burying interlayer films between wiring layers, and decreasing absolute steps.

SOLUTION: An insulating film 12, a titan film 14 and a titan nitride film 16 as a first barrier film, a copper film 18, a titan nitride film 20 as a second barrier film, and a silicon nitride film 22 as a film for forming an etching mask are sequentially laminated on a silicon substrate 10, and a photoresist 24 is coated thereon, and a wiring pattern is formed by a photolithography technique, and the silicon nitride film 22 is etched using the photoresist 24 as an etching mask to form an etching mask 22. After the photoresist 24 is removed by ashing wiring layer is formed by etching using the etching mask 22, and the etching mask 22 is removed by etching, and immersed in a benzotriazol liquid to form a Cu-BTA (benzotriazole) compound 26 at the sidewall of the copper film 18. And an interlaminar insulating film 28 is formed to obtain the copper wiring of low resistance and high reliability.



LEGAL STATUS

CLAIMS

[Claim(s)]

[Claim 1] The manufacture method of the semiconductor device which forms the element which used copper as a wiring material on a semiconductor substrate characterized by providing the following. The process which forms an insulator layer on the aforementioned substrate. The process which carries out laminating formation of the 1st barrier film, a copper film, and the 2nd barrier film one by one on the aforementioned insulator layer. The process which forms the film for etching mask formation on the barrier film of the above 2nd. The process which applies a sensitization agent on the film for the aforementioned etching mask formation, and the process which exposes the aforementioned sensitization agent alternatively and forms a predetermined circuit pattern at a sensitization agent, The process which **********s the film for the aforementioned etching mask formation by using as a mask the aforementioned sensitization agent in which the circuit pattern was formed, and forms an etching mask, The process which removes the aforementioned sensitization agent, and the process which **********s the barrier film of the above 1st, a copper film, and the 2nd barrier film using the aforementioned etching mask, and forms a wiring layer, The process which removes the aforementioned etching mask, the process which forms the layer of the wiring layer of the aforementioned copper which prevents oxidization and diffusion on a side attachment wall at least, and the process which forms a wrap protective coat for the aforementioned whole wiring layer.

[Claim 2] The manufacture method of the semiconductor device which forms the element which used copper as a wiring material on a semiconductor substrate characterized by providing the following. The process which forms an insulator layer on the aforementioned substrate. The process which carries out laminating formation of the 1st barrier film, a copper film, and the 2nd barrier film one by one on the aforementioned insulator layer. The process which forms the film for etching mask formation on the barrier film of the above 2nd. The process which applies a sensitization agent on the film for the aforementioned etching mask formation, and the process which exposes the aforementioned sensitization agent alternatively and forms a predetermined circuit pattern at a sensitization agent, The process which **********s the film for the aforementioned etching mask formation by using as a mask the aforementioned sensitization agent in which the circuit pattern was formed, and forms an etching mask, The process which removes the aforementioned sensitization agent, and the process which **********s the barrier film of the above 1st, a copper film, and the 2nd barrier film using the aforementioned etching mask, and forms a wiring layer, The process which removes the aforementioned etching mask and the barrier film of the above 2nd, the process which forms the layer which prevents oxidization and diffusion on the upper surface and the side attachment wall of a wiring layer of the aforementioned copper, and the process which forms a wrap protective coat for the aforementioned whole wiring layer.

[Claim 3] The manufacture method of a semiconductor device according to claim 1 or 2 that the barrier film of the above 1st and the 2nd barrier film are characterized by being a silicon nitride, an acid silicon nitride, a titanium nitride, a nitriding tungsten, a titanium-nitride tungsten, a tungsten, niobium, niobium nitride, aluminum, a tantalum, or a tantalum nitride.

[Claim 4] The manufacture method of a semiconductor device according to claim 1 or 2 that the film for the aforementioned etching mask formation is characterized by being a silicon nitride, a silicon oxide, or an acid silicon nitride.

[Claim 5] The manufacture method of the semiconductor device according to claim 1 or 2 characterized by being the membrane type from which the film for the aforementioned etching mask formation and the barrier film of the above 2nd differ.

[Claim 6] The manufacture method of the semiconductor device according to claim 1 or 2 characterized by leaving the barrier film of the above 2nd at the process which **********s the film for the aforementioned etching mask formation, and forms an etching mask.

[Claim 7] The etching gas used at the process which **********s the film for the aforementioned etching mask formation, and forms an etching mask is the manufacture method of the claim 1

characterized by including the compound expressed with CnHmF (2n+2-m), and a semiconductor device according to claim 2 or 6.
[Claim 8] The etching conditions used at the process which **********s the film for the aforementioned etching mask formation, and forms an etching mask are the manufacture method of the claim 1 characterized by making the etch rate of the barrier film of the above 2nd later than the etch rate of the film for the aforementioned etching mask formation, a claim 2, and a semiconductor device according to claim 6 or 7.
[Claim 9] The etching gas used at the process which **********s the barrier film of the above 1st, the 2nd barrier film, and a copper film using the aforementioned etching mask, and forms a wiring layer is the manufacture method of the semiconductor device according to claim 1 or 2 characterized by being gas containing chlorine.
[Claim 10] The etching gas used at the process which removes the aforementioned etching mask is the manufacture method of the semiconductor device according to claim 1 characterized by containing the compound expressed with CnHmF (2n+2-m).
[Claim 11] The etching gas used at the process which removes the aforementioned etching mask and the barrier film of the above 2nd is the manufacture method of the semiconductor device according to claim 2 characterized by containing 6 sulfur fluoride.
[Claim 12] The etching conditions used at the process which removes the aforementioned etching mask are the manufacture method of the semiconductor device according to claim 1 or 10 characterized by making the etch rate of the 2nd aforementioned barrier film later than the etch rate of the film of the aforementioned etching mask.
[Claim 13] The etching conditions used at the process which removes the barrier film of the aforementioned etching mask and the above 2nd are the manufacture method of the semiconductor device according to claim 2 or 11 characterized by making almost equal the etch rate of the film for the aforementioned etching mask formation, and the etch rate of the barrier film of the above 2nd.
[Claim 14] The process which forms the layer of the wiring layer of the aforementioned copper which prevents oxidization and diffusion on a side attachment wall at least is the manufacture method of the semiconductor device according to claim 1 or 2 characterized by processing the aforementioned wiring layer front face in gas atmosphere.
[Claim 15] The process which forms the layer of the wiring layer of the aforementioned copper which prevents oxidization and diffusion on a side attachment wall at least is the manufacture method of the semiconductor device according to claim 1 or 2 characterized by carrying out solution processing of the aforementioned wiring layer front face.
[Claim 16] The process which forms the layer of the wiring layer of the aforementioned copper which prevents oxidization and diffusion on a side attachment wall at least is a semiconductor device according to claim 1 or 2 characterized by pouring in an impurity into the aforementioned wiring layer.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture method of a semiconductor device, and relates to the manufacture method of the semiconductor device which forms in more detail the element which used copper as a wiring material on the semiconductor substrate.
[0002]
[Description of the Prior Art] Conventionally, integrated circuits, such as IC and LSI which formed many elements and wiring with high density on the semiconductor substrate, or a VLSI, are manufactured. In this kind of semiconductor device, in order to realize the further improvement in the speed and the further large-capacity-izing, the degree of integration needed to be raised. However, since reduction of the wiring width of face accompanying this high integration leads to high resistance-ization, it is desirable to use what has resistance small as much as possible as a wiring material. For this reason, recently, it replaces with aluminum etc. and the semiconductor device using the copper which is low electrical resistance materials as a wiring material is proposed.
[0003] Then, a part of manufacturing process of the conventional semiconductor device at the time of using copper as a wiring material is shown in (a) - (c) of drawing 5 . Here, in order to simplify explanation, the explanation about the formation method of a transistor portion is omitted.
[0004] As shown in drawing 5 (a), in order to separate a transistor portion and a wiring layer, on a silicon substrate 50, an insulator layer 52 is formed by the CVD (Chemical Vaper Deposition : chemical vapor deposition) method. And on the insulator layer 52, the titanium film (Ti) 54 was formed by the sputtering method, the titanium-nitride film (TiN) 56 was formed by the reactive-sputtering method or the RTA (Rapid Thermal Anneal) method on it, and the copper film (Cu) 58 was further formed of the sputtering method or CVD on it.
[0005] As shown in drawing 5 (b), after applying the about 1.0-micrometer photoresist 60 on the copper film (Cu) 58 and forming this in a desired circuit pattern with photolithography technology next, the wiring layer was formed by **********ing by the reactive-ion-etching (RIE) method by making this into an etching mask. As etching gas used in case this reactive ion etching is performed, a silicon tetrachloride (SiCl4), nitrogen (N2), and the argon (Ar) were used, for example. Moreover, the temperature of a silicon substrate 50 was low, and since the etch rate was slow, the vapor pressure of the chloride of the copper generated by etching made it about [300 degrees] C. And after removing a photoresist 60 by the oxygen ashing method, as shown in drawing 5 (c), the insulator layer 62 as layer mesenteriolum which embeds between wiring layers was formed.
[0006]
[Problem(s) to be Solved by the Invention] However, if it was in the manufacture method of such a conventional semiconductor device, there was un-arranging [that the electric resistance of a copper film 58 rose according to the process which removes a photoresist 60 by oxygen ashing, and the process which forms an insulator layer 62]. This is considered to be because for a copper oxide to be formed of the inside of a hot oxygen atmosphere, or oxygen plasma in case an insulator layer 62 is formed by the plasma CVD method etc., that the front face of a copper film 58 oxidizes by the oxygen plasma or ozone used for ashing, and. namely, the inclination for wiring width of face to become thin by integration since a copper oxide (for example, Cu2 O, CuO) has high electric resistance, copper oxidization is diffused inside unlike an alumina (aluminum oxide : aluminum 2O3) and it is promoted -- in addition, when copper oxidization progressed, it was un-arranging [that the whole wiring resistance went up] at a stretch
[0007] Then, various methods are proposed in order to prevent oxidization of copper wiring. For example, having un-arranged [that the oxidization from a side attachment wall tends to take place, and the total thickness of a wiring layer becomes thick, and the embedding of a layer insulation film becomes difficult], since this method was taken into consideration only about oxidization on the front face of copper, although the method of forming an antioxidizing film in the front face of copper wiring

was proposed according to ** JP,63-174336,A.
[0008] Moreover, according to the official reports, such as ** JP,62-290150,A, JP,63-73645,A, JP,63-156341,A, JP,6-275620,A, JP,6-275621,A, and JP,6-130743,A, in order to prevent not only the front face of copper wiring but the oxidization from a side attachment wall, the method of forming an antioxidizing film to the whole substrate after copper wiring formation is proposed. However, by these methods, since the oxidization at the time of ashing which was mentioned above was not taken into consideration, it was not practical, and since the antioxidizing film was formed after forming copper wiring, it could not apply to a detailed pattern, but there was un-arranging [that the embedding of the layer mesenteriolum became difficult] further.
[0009] Then, by each of such technique, since oxidization of a copper film is surely caused at the time of ashing, the method of returning the copper oxide which oxidized at the time of ashing, and making it into a copper film is also proposed by adding heat treatment in the atmosphere containing ** hydrogen. However, although hydrogen was returned to copper (Cu) by this method by the reaction which carries out a diffusion invasion into a copper film (Cu2 O+H2 ->2 Cu+H2 O), since a steam was generated simultaneously with this, the foam and the crack occurred in the copper film with the generated steam, and there was un-arranging [of having degraded membraneous quality].
[0010] Then, in order to make it oxidization not take place at the time of ashing, according to ** JP,6-244181,A, first, the film of another composition element is formed on the film which prevents oxidization of the copper upper surface, a hard surface mask blank is formed, patterning of the copper cascade screen is carried out [patterning of this film is carried out by the resist,] by the aforementioned hard surface mask blank after resist removal, and the method of forming a layer insulation film at the upper part is proposed. However, by this method, the thickness of the layer mesenteriolum required for embedding having also un-arranged [of becoming thick], since the thickness of a circuit pattern became thick by forming a hard surface mask blank even if it can prevent the oxidization at the time of ashing. namely, -- if the thickness of the layer mesenteriolum becomes thick -- connection -- the depth of a hole -- deep -- becoming -- the connection -- since the time which etching for forming a hole takes becomes long, a throughput falls and a size controllability also becomes bad Moreover, if the thickness of a circuit pattern becomes thick, it will become easy to generate the cavity called a void (Void) between wiring at the time of layer mesenteriolum formation. Furthermore, the more it became difficult to carry out flattening and it became the upper wiring even if it formed the layer mesenteriolum since a level difference increased absolutely when the thickness of a circuit pattern became thick, the more there was un-arranging [that exposure became difficult].
[0011] the time of exposure [in / the upper wiring / by preventing the diffusion to an insulator from copper, and the diffusion of an impurity to copper, and embedding the layer mesenteriolum proper between wiring, while took an example inconvenient, it was made and this invention prevents / which this conventional technology has / oxidization of copper wiring] -- absolutely -- a level difference -- decreasing -- low resistance -- high -- aiming at acquiring the manufacture method of the semiconductor device equipped with reliable copper wiring
[0012]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, invention according to claim 1 The process which is the manufacture method of the semiconductor device which forms the element which used copper as a wiring material on a semiconductor substrate, and forms an insulator layer on the aforementioned substrate, The process which carries out laminating formation of the 1st barrier film, a copper film, and the 2nd barrier film one by one on the aforementioned insulator layer, The process which forms the film for etching mask formation on the barrier film of the above 2nd, The process which applies a sensitization agent on the film for the aforementioned etching mask formation, and the process which exposes the aforementioned sensitization agent alternatively and forms a predetermined circuit pattern at a sensitization agent, The process which **********s the film for the aforementioned etching mask formation by using as a mask the aforementioned sensitization agent in which the circuit pattern was formed, and forms an etching mask, The process which removes the aforementioned sensitization agent, and the process which **********s the barrier film of the above

1st, a copper film, and the 2nd barrier film using the aforementioned etching mask, and forms a wiring layer, It has at least the process which removes the aforementioned etching mask, the process which forms the layer of the wiring layer of the aforementioned copper which prevents oxidization and diffusion on a side attachment wall at least, and the process which forms a wrap protective coat for the aforementioned whole wiring layer.

[0013] According to this, the vertical side of a copper film can be protected from oxidization etc. by the barrier film by carrying out laminating formation of the 1st barrier film, a copper film, and the 2nd barrier film one by one, **********ing this, and forming a wiring layer on an insulator layer. Since a sensitization agent is used, an etching mask is formed and it etches with this etching mask (called a hard surface mask blank) in case a sensitization agent like a photoresist is not used as a direct etching mask but patterning of the film for etching mask formation is carried out, when forming a wiring layer by this etching, oxidization of the copper by ashing used in case a sensitization agent is removed can be prevented. Moreover, since it is removed after forming a wiring layer by etching and the total thickness of a circuit pattern does not increase, the embedding property at the time of embedding a protective coat to between wiring is not spoiled, but this etching mask can suppress generating of a void etc. Since an etching mask can moreover be constituted thickly, it becomes possible to take the large margin of the etching conditions of a wiring layer. since [furthermore,] thickness of a protective coat required for embedding can be made thin -- connection -- the time which etching takes by the depth of a hole becoming shallow -- short -- becoming -- a throughput -- improving -- the connection -- it becomes good [the size controllability of a hole] Moreover, if the thickness of a circuit pattern is reduced, since a level difference can be absolutely made small, the large margin of the exposure conditions of the upper wiring can be taken. since [thus,] oxidization etc. can form the copper wiring which can be prevented certainly on a semiconductor substrate -- low resistance -- high -- a reliable semiconductor device can be manufactured

[0014] The process which invention according to claim 2 is the manufacture method of the semiconductor device which forms the element which used copper as a wiring material on a semiconductor substrate, and forms an insulator layer on the aforementioned substrate, The process which carries out laminating formation of the 1st barrier film, a copper film, and the 2nd barrier film one by one on the aforementioned insulator layer, The process which forms the film for etching mask formation on the barrier film of the above 2nd, The process which applies a sensitization agent on the film for the aforementioned etching mask formation, and the process which exposes the aforementioned sensitization agent alternatively and forms a predetermined circuit pattern at a sensitization agent, The process which **********s the film for the aforementioned etching mask formation by using as a mask the aforementioned sensitization agent in which the circuit pattern was formed, and forms an etching mask, The process which removes the aforementioned sensitization agent, and the process which **********s the barrier film of the above 1st, a copper film, and the 2nd barrier film using the aforementioned etching mask, and forms a wiring layer, It has at least the process which removes the aforementioned etching mask and the barrier film of the above 2nd, the process which forms the layer which prevents oxidization and diffusion on the upper surface and the side attachment wall of a wiring layer of the aforementioned copper, and the process which forms a wrap protective coat for the aforementioned whole wiring layer.

[0015] According to this, after in addition to an operation of the above-mentioned invention according to claim 1 **********ing and forming a wiring layer using an etching mask, the 2nd barrier film is also removed with an etching mask. for this reason -- while it becomes possible to make the film of a wiring layer still thinner and the embedding property of the protective coat which embeds between wiring layers becomes much more good -- the thickness of a protective coat -- thin -- it can carry out -- connection -- the depth of a hole becomes shallow, the time which etching takes becomes short, and a throughput is improved -- making -- connection -- the size controllability of a hole can be made good Moreover, if the thickness of a wiring layer is reduced, a level difference becomes still smaller absolutely and the still larger margin of the exposure conditions of the upper wiring can be taken. since [thus,] oxidization etc. can form the copper wiring which can be prevented certainly on a

semiconductor substrate -- low resistance -- high -- a reliable semiconductor device can be manufactured

[0016] Invention according to claim 3 is characterized by the barrier film of the above 1st and the 2nd barrier film being a silicon nitride, an acid silicon nitride, a titanium nitride, a nitriding tungsten, a titanium-nitride tungsten, a tungsten, niobium, niobium nitride, aluminum, a tantalum, or a tantalum nitride in the manufacture method of a semiconductor device according to claim 1 or 2.
[0017] Since the 1st barrier film and the 2nd barrier film are formed of the quality of the material which prevents oxidization of copper wiring according to this, oxidization of copper wiring can be certainly prevented with these barrier films.
[0018] Invention according to claim 4 is characterized by the film for the aforementioned etching mask formation being a silicon nitride, a silicon oxide, or an acid silicon nitride in the manufacture method of a semiconductor device according to claim 1 or 2.
[0019] According to this, since it consists of the quality of the material which constitutes the so-called hard surface mask blank, ashing at the time of removing an etching mask becomes unnecessary, and the film with which an etching mask is formed can prevent oxidization of the copper film at the time of ashing. Moreover, it enables it to form an etching mask certainly by considering as the quality of the material which etch selectivity tends to take between the 2nd barrier film at the time of etching at the time of forming an etching mask.
[0020] Invention according to claim 5 is characterized by being the membrane type from which the film for the aforementioned etching mask formation and the barrier film of the above 2nd differ in the manufacture method of a semiconductor device according to claim 1 or 2.
[0021] Since the film for etching mask formation and the 2nd barrier film were formed with a different membrane type according to this, in case the film for etching mask formation is **********ed and an etching mask is formed, it becomes possible to take etch selectivity, and an etching mask can be formed certainly.
[0022] In the manufacture method of a semiconductor device according to claim 1 or 2, invention according to claim 6 is the process which **********s the film for the aforementioned etching mask formation, and forms an etching mask, and is characterized by leaving the barrier film of the above 2nd.
[0023] In case the film for etching mask formation is **********ed by using sensitization agents, such as a photoresist, as a mask according to this, when even the 2nd barrier film under it carries out over etching, an etching mask can be formed certainly. Since it **********s in that case so that it may leave the 2nd barrier film, even if it carries out ashing removal of the sensitization agent, oxidization of a copper film can be prevented.
[0024] The etching gas used at the process which invention according to claim 7 **********s the film for the aforementioned etching mask formation in the manufacture method of a claim 1 and a semiconductor device according to claim 2 or 6, and forms an etching mask is characterized by including the compound expressed with CnHmF (2n+2-m).
[0025] Since according to this the etching gas containing the compound expressed with CnHmF (2n+2-m) is used in case the film for etching mask formation is **********ed, patterning of the film for etching mask formation can be carried out certainly, and an etching mask can be formed.
[0026] The etching conditions used at the process which invention according to claim 8 **********s the film for the aforementioned etching mask formation in the manufacture method of a claim 1, a claim 2, and a semiconductor device according to claim 6 or 7, and forms an etching mask are characterized by making the etch rate of the barrier film of the above 2nd later than the etch rate of the film for the aforementioned etching mask formation.
[0027] According to this, as etching conditions, the etch rate of the 2nd barrier film can be written late, it can leave the 2nd barrier film, patterning of the film for etching mask formation can be carried out certainly, and an etching mask can be formed rather than the speed which **********s the film for etching mask formation.
[0028] The etching gas used at the process which invention according to claim 9 **********s the barrier film of the above 1st, the 2nd barrier film, and a copper film using the aforementioned etching

mask in the manufacture method of a semiconductor device according to claim 1 or 2, and forms a wiring layer is characterized by being gas containing chlorine.
[0029] It is 3 (CrCl) by using the gas containing chlorine, in case it **********s at the process which forms a wiring layer according to this. Since vapor pressure is higher than the vapor pressure of copper halogenides, such as other gas (for example, F, I), copper wiring can be formed certainly.
[0030] The etching gas by which invention according to claim 10 is used at the process which removes the aforementioned etching mask in the manufacture method of a semiconductor device according to claim 1 is characterized by containing the compound expressed with CnHmF (2n+2-m).
[0031] In the process which removes an etching mask, by **********ing using the etching gas by which the compound expressed with CnHmF (2n+2-m) was contained, it can leave the 2nd barrier film and, according to this, an etching mask can be removed certainly.
[0032] The etching gas by which invention according to claim 11 is used at the process which removes the aforementioned etching mask and the barrier film of the above 2nd in the manufacture method of a semiconductor device according to claim 2 is characterized by containing 6 sulfur fluoride.
[0033] According to this, in the process which removes an etching mask and the 2nd barrier film, it becomes possible to remove an etching mask and the 2nd barrier film certainly by **********ing using the etching gas by which 6 sulfur fluoride (CF6) is contained. And if an etching mask and the 2nd barrier film are removed certainly, thickness of the whole wiring layer can be made thin, embedding during wiring by the protective coat etc. will be performed proper, and it will be hard coming to generate a void between wiring. moreover -- if it becomes thin about the thickness of a protective coat required for embedding -- connection -- the depth of a hole becomes shallow, the time which etching takes becomes short, and a throughput is improved -- it can make -- connection -- it becomes good [the size controllability of a hole] Moreover, if the thickness of a wiring layer is reduced, since a level difference can be absolutely made small, the large margin of the exposure conditions of the upper wiring can be taken.
[0034] Invention according to claim 12 is characterized by the etching conditions used at the process which removes the aforementioned etching mask making the etch rate of the 2nd aforementioned barrier film later than the etch rate of the film of the aforementioned etching mask in the manufacture method of a semiconductor device according to claim 1 or 10.
[0035] According to this, as etching conditions, the etch rate of the 2nd barrier film can be written late, it leaves the 2nd barrier film, and it **********s certainly and only an etching mask can be removed from the etch rate of an etching mask.
[0036] The etching conditions for which invention according to claim 13 is used at the process which removes the barrier film of the aforementioned etching mask and the above 2nd in the manufacture method of a semiconductor device according to claim 2 or 11 are characterized by making almost equal the etch rate of the film for the aforementioned etching mask formation, and the etch rate of the barrier film of the above 2nd.
[0037] According to this, an etching mask and the 2nd barrier film are certainly removable as etching conditions by having made almost equal the etch rate of the film for etching mask formation, and the etch rate of the 2nd barrier film.
[0038] The process in which invention according to claim 14 forms the layer of the wiring layer of the aforementioned copper which prevents oxidization and diffusion on a side attachment wall at least in the manufacture method of a semiconductor device according to claim 1 or 2 is characterized by processing the aforementioned wiring layer front face in gas atmosphere.
[0039] According to this, the layer of a copper wiring layer which prevents oxidization and diffusion on a side attachment wall at least can be formed by processing a wiring layer front face in gas atmosphere.
[0040] The process in which invention according to claim 15 forms the layer of the wiring layer of the aforementioned copper which prevents oxidization and diffusion on a side attachment wall at least in the manufacture method of a semiconductor device according to claim 1 or 2 is characterized by carrying out solution processing of the aforementioned wiring layer front face.
[0041] According to this, the layer of a copper wiring layer which prevents oxidization and diffusion on

a side attachment wall at least can be formed by carrying out solution processing of the wiring layer front face.
[0042] The process in which invention according to claim 16 forms the layer of the wiring layer of the aforementioned copper which prevents oxidization and diffusion on a side attachment wall at least in a semiconductor device according to claim 1 or 2 is characterized by pouring in an impurity into the aforementioned wiring layer.
[0043] According to this, the layer of a copper wiring layer which prevents oxidization and diffusion on a side attachment wall at least can be formed by pouring in an impurity into a wiring layer.
[0044]
[Embodiments of the Invention] Hereafter, the gestalt of implementation of the manufacture method of the semiconductor device concerning this invention is explained based on a drawing.
[0045] (Gestalt 1 of operation) It is the process cross section which explains the manufacture method of the semiconductor device concerning the gestalt 1 of operation to drawing 1 . In drawing 1 (a), the insulator layer 12 for separating a transistor portion and a wiring layer is formed by the CVD (Chemical Vaper Deposition) method on a silicon substrate 10.
[0046] Next, on an insulator layer 12, the titanium film (Ti) 14 and the titanium-nitride film (TiN) 16 as 1st barrier film are formed. Subsequently, a copper film (Cu) 18 is formed on the titanium-nitride film (TiN) 16, and the titanium nitride (TiN) 20 as 2nd barrier film is formed one by one on it. Here, the titanium-nitride film (TiN) 20 is formed of the CVD using the material gas containing the reactive-sputtering method or nitrogen in the inside of nitrogen atmosphere by forming the titanium film (Ti) 14 of the sputtering method or CVD, and a copper film (Cu) 18 is formed of the sputtering method or CVD. This copper film 18 may not be limited to a pure copper, may contain some other elements, and may be a copper alloy.
[0047] Each above-mentioned thickness at this time is not necessarily limited to such thickness, although 150A and the titanium-nitride film (TiN) 16 were formed for the titanium film (Ti) 14 and 5000A and the titanium-nitride film 20 were formed for 800A and the copper film (Cu) 18 as 800A here. Moreover, as a film for etching mask formation used as an etching mask at a next process, a silicon nitride film (SiN) 22 is formed here, and the thickness may be about 3000A.
[0048] On a silicon substrate 10, thus, an insulator layer 12, the 1st barrier film [the titanium film (Ti) 14 and the titanium-nitride film (TiN) 16], After carrying out laminating formation of a copper film (Cu) 18, the 2nd barrier film [the titanium-nitride film (TiN) 20], and the film for etching mask formation [a silicon nitride film (SiN) 22] one by one, as shown in drawing 1 (b) On a silicon nitride (SiN) 22, a photoresist 24 is applied to the thickness of about 1.0 micrometers, and a desired circuit pattern is formed using photolithography technology.
[0049] And the film for the aforementioned etching mask formation [a silicon nitride film (SiN) 22] is **********ed by using a photoresist 24 as a mask by the reactive-ion-etching (RIE) method, and this forms the etching mask 22. As etching gas at this time, it is CF4. H2 It uses and **********s by reactive ion etching. The quantity of gas flow in that case is CF4. It is 25 (SCCM) and is H2. It is 15 (SCCM). Moreover, when RF power at the time of etching is set to 400 (W) and gas pressure is set to 5 (mTorr), the etch-rate ratio of a silicon nitride (SiN) 22 and the titanium-nitride film (TiN) 20 which is a hard surface mask blank is set to SiN/TiN=6. For this reason, since the titanium-nitride film (TiN) 20 is not lost even if it performs over etching, in order to carry out patterning of the silicon nitride (SiN) 22 certainly, it leaves the titanium-nitride film (TiN) 20 which is the 2nd barrier film, a silicon nitride (SiN) 22 is **********ed, and an etching mask can be formed certainly.
[0050] Next, a photoresist 24 is removed by ashing as shown in drawing 1 (c). Since the titanium nitride (TiN) 20 which is the 2nd barrier film in the front face of a copper film (Cu) 18 at this time has covered, it does not oxidize.
[0051] Next, as shown in drawing 1 (d), wiring is formed by using a silicon nitride film (SiN) 22 as an etching mask by the reactive-ion-etching (RIE) method by **********ing even the titanium-nitride film (TiN) 20 - the titanium film (Ti) 14. As etching gas at this time, chlorine (Cl2), a silicon tetrachloride (SiCl4), nitrogen (N2), and an argon (Ar) are used. And 25 (SCCM) and nitrogen (N2) are setting to 100

(SCCM), and the argon (Ar) is setting [chlorine (Cl2) / 25 (SCCM) and the silicon tetrachloride (SiCl4)] the quantity of gas flow here to 50 (SCCM). Moreover, RF power at the time of etching is set to 400 (W), and is setting the pressure to 15 (mTorr). Moreover, the temperature of a silicon substrate is low, and since the etch rate is slow, the vapor pressure of the chloride of the copper generated by etching makes it about [300 degrees] C. In this case, each etch-rate ratio with the silicon nitride (SiN) 22 which is a hard surface mask blank, copper (Cu), and the titanium-nitride film (TiN) 20 is set to SiN/TiN**10 and SiN/Cu**10.

[0052] Next, as shown in drawing 1 (e), the film for etching mask formation [a silicon nitride film (SiN) 22] mentioned above is removed. At this time, it is CF4 as etching gas. H2 It used and etched by reactive ion etching. The quantity of gas flow in that case is CF4. 25 (SCCM) H2 It is 15 (SCCM). Moreover, when RF power is set to 400 (W) and a pressure is set to 5 (mTorr), the ratio of the etch rate of the silicon nitride (SiN) 22 and the titanium-nitride film (TiN) 20 which are a hard surface mask blank can be written as SiN/TiN=6, can leave the titanium-nitride film (TiN) 20 which is the 2nd barrier film, and can remove certainly the film for etching mask formation [a silicon nitride (SiN) 22]. Thus, since the film for etching mask formation is finally removed and it can form the thickness of the film for etching mask formation thickly, it can extend the margin of the etching conditions at the time of circuit pattern formation.

[0053] Next, in drawing 1 (f), the silicon wafer which forms a semiconductor device is dipped in the solution containing the benzotriazol (BTA). Since the insoluble Cu-BTA compound 26 is formed in the front face (side attachment wall) of a copper film (Cu) 18 at this time, the barrier layer which prevents copper oxidization can be formed.

[0054] The layer insulation film 28 as a protective coat which protects a wiring layer is formed at the same time it next embeds between wiring layers, as shown in drawing 1 (g).

[0055] Since it is covered with the Cu-BTA compound 26, the front face of a copper film (Cu) 18 does not oxidize to the interior of wiring, but can be prevented from causing resistance elevation according to the gestalt 1 of operation, as explained above.

[0056] Moreover, in order to remove an etching mask [a silicon nitride (SiN) 22] here, thickness of the whole wiring layer can be made thin, it is lost that the embedding property of a between [wiring of the layer insulation film 28] is spoiled, and it is hard coming to generate a void between wiring. if the thickness of the whole wiring layer becomes thin, since [furthermore,] thickness of the layer mesenteriolum required for embedding can be made thin -- connection -- the depth of a hole becomes shallow, the time which etching takes becomes short, and a throughput is improved -- it can make -- connection -- the size controllability of a hole also becomes good Moreover, since the silicon nitride (SiN) 22 which is a hard surface mask blank is finally removed, it is possible to form a hard surface mask blank thickly, and the large margin of the etching conditions at the time of circuit pattern formation (selection ratio of a hard surface mask blank and a wiring layer) can be taken. Moreover, since a level difference will become small absolutely if the total thickness of wiring is reduced as mentioned above, the margin of the exposure conditions of the upper wiring can be extended.

[0057] (Gestalt 2 of operation) Below, the gestalt 2 of operation of this invention is explained based on drawing 2 . Here, about a component the same as that of the gestalt 1 of operation mentioned above, or equivalent, while attaching the same sign, simple [of the explanation] shall be carried out, or it shall omit.

[0058] The manufacturing process of the semiconductor device of the gestalt 2 of operation shown in drawing 2 is the process that drawing 1 (d) is the same, and shows the process after (e) of drawing 1 by drawing 2 (a) - (c). For this reason, only a process characteristic of the gestalt 2 of operation is explained using drawing 2 .

[0059] In drawing 1 (d) mentioned above, after **********ing even the titanium-nitride film (TiN) 20 - the titanium film (Ti) 14 using the etching mask 22, as shown in drawing 2 (a), the feature of the gestalt 2 of operation is that it carries out etching removal of the etching mask 22 and the titanium-nitride film (TiN) 20 which is the 2nd barrier film simultaneously by RIE. As etching gas used in case etching removal of this etching mask 22 and the 2nd barrier film 20 is carried out, the gas by which 6 sulfur

fluoride (SF6) was contained here is used. Moreover, the quality of the material is chosen so that the etch rate of the etching mask 22 and the 2nd barrier film 20 may become almost equal as the etching condition.
[0060] By dipping a silicon wafer in the solution containing the benzotriazol (BTA), after removing simultaneously the etching mask 22 and the 2nd barrier film 20 as mentioned above, as shown in drawing 2 (b), the Cu-BTA compound 26 can be formed in the front face (the upper surface and side attachment wall) of a copper film (Cu) 18, and the barrier layer which protects so that the front face of a copper film 18 may not oxidize by this is formed.
[0061] The layer insulation film 28 as a protective coat which protects a wiring layer is formed at the same time it next embeds between wiring layers, as shown in drawing 2 (c).
[0062] Since the front face (the upper surface and side attachment wall) of a copper film (Cu) 18 is being worn with the Cu-BTA compound 26 according to the gestalt 2 of operation as explained above, oxidizing to the interior of wiring is lost and it can avoid causing resistance elevation. Moreover, since the etching mask 22 and the 2nd barrier layer 20 were removed, it becomes possible to make thickness of a wiring layer still thinner, the embedding property of a between [wiring of the layer insulation film 28] becomes good, and it is hard coming to generate a void between wiring. since [furthermore,] thickness of the layer mesenteriolum required for embedding can also be made still thinner -- connection -- the depth of a hole becomes shallow, the time which etching takes becomes short, and a throughput is improved further -- it can make -- connection -- it becomes good [the size controllability of a hole]
[0063] Moreover, also in the gestalt 2 of operation, in order to remove a hard surface mask blank finally, it is thickly possible a hard surface mask blank, and the large margin of the etching conditions at the time of circuit pattern formation (etch selectivity of a hard surface mask blank and a wiring layer) can be taken.
[0064] Moreover, in the case of the gestalt 2 of operation, since the total thickness of a wiring layer can decrease further and can make a level difference small absolutely, the margin of the exposure conditions of the upper wiring can be extended.
[0065] (Gestalt 3 of operation) Below, the gestalt 3 of operation of this invention is explained based on drawing 3 . Here, about a component the same as that of the gestalten 1 and 2 of operation mentioned above, or equivalent, while attaching the same sign, simple [of the explanation] shall be carried out, or it shall omit.
[0066] The manufacturing process of the semiconductor device of the gestalt 3 of operation shown in drawing 3 is the process that drawing 1 (e) is the same, and shows the process after (f) of drawing 1 by drawing 3 (a) and (b). For this reason, only a process characteristic of the gestalt 3 of operation is explained using drawing 3 .
[0067] In drawing 1 (e) mentioned above, after removing the film for etching mask formation, as shown in drawing 3 (a), the feature of the gestalt 3 of operation is that it forms the barrier layer which prevents oxidization and diffusion by processing the aforementioned wiring layer front face in gas atmosphere. The gas by which the silane (SiH4) was contained as gas used in case this wiring layer front face is processed in gas atmosphere is used. A substrate is heated at about 300 degrees C, by passing silane gas in a vacuum housing, copper and silane gas cause solid phase-gaseous phase reaction, and the silicide 30 of thin copper is formed in a front face. The barrier layer which protects so that the front face of a copper film 18 may not oxidize by this is formed.
[0068] The layer insulation film 28 as a protective coat which protects a wiring layer is formed at the same time it next embeds between wiring layers, as shown in drawing 3 (b).
[0069] Since the front face of a copper film (Cu) 18 is being worn by the silicide according to the gestalt 3 of operation as explained above, oxidizing to the interior of wiring is lost and it can avoid causing resistance elevation. Moreover, although the layer which prevents oxidization and diffusion is formed in the front face of a copper wiring layer, since it processes in gas atmosphere, it can carry out in a vacuum housing continuously with the removal process of the film for etching mask formation and formation of a natural oxidation film is barred, elevation of resistance can be inhibited further.
[0070] In addition, although the gestalt 3 of above-mentioned operation showed the method which

removed only the etching mask 22, the method which removed simultaneously the etching mask 22 and the 2nd barrier film 20 like the gestalt 2 of operation may be used, and it does not limit to this.
[0071] Moreover, as gas which carries out atmosphere processing, although the silane was shown, it does not limit to this. For example, a disilane is sufficient.
[0072] Moreover, although the copper silicide was shown as matter formed of processing of gas atmosphere, it does not limit to this that what is necessary is just what prevents copper oxidization.
[0073] (Gestalt 4 of operation) Below, the gestalt 4 of operation of this invention is explained based on drawing 4 . Here, about a component the same as that of the gestalten 1, 2, and 3 of operation mentioned above, or equivalent, while attaching the same sign, simple [of the explanation] shall be carried out, or it shall omit.
[0074] The manufacturing process of the semiconductor device of the gestalt 4 of operation shown in drawing 4 is the process that drawing 1 (e) is the same, and shows the process after (f) of drawing 1 by drawing 4 (a) and (b). For this reason, only a process characteristic of the gestalt 4 of operation is explained using drawing 4 .
[0075] In drawing 1 (e) mentioned above, after removing the film for etching mask formation, as shown in drawing 4 (a), silicon (Si) is injected into the side attachment wall of the aforementioned wiring layer with ion-implantation, and the feature of the gestalt 4 of operation is that it forms the barrier layer which prevents oxidization and diffusion. In addition, at this time, to the pouring direction of silicon, it is not perpendicular, and the semiconductor substrate in which the wiring layer was formed is leaned to the angle of about about 5 degrees, and is rotated. Silicon is injected very much also into the side attachment wall of wiring on a front face by this.
[0076] By heat-treating in oxygen or nitrogen atmosphere, it becomes the copper silicide 32 and barrier nature of the front face of a copper film 18 improves to oxidization or a nitriding pan, and a pan at the next.
[0077] The layer insulation film 28 as a protective coat which protects a wiring layer is formed at the same time it next embeds between wiring layers, as shown in drawing 4 (b).
[0078] Since the front face of a copper film (Cu) 18 is being worn by the silicide according to the gestalt 4 of operation as explained above, oxidizing to the interior of wiring is lost and it can avoid causing resistance elevation.
[0079] In addition, although the gestalt 4 of above-mentioned operation showed the method which removed only the etching mask 22, the method which removed simultaneously the etching mask 22 and the 2nd barrier film 20 like the gestalt 2 of operation may be used, and it does not limit to this.
[0080] Moreover, as an ion kind to pour in, although silicon was shown, it does not limit to this.
[0081] Moreover, although the copper silicide was shown as matter formed by the ion implantation, it does not limit to this that what is necessary is just what prevents copper oxidization.
[0082] In addition, with the gestalt of each operation mentioned above, as 1st barrier film, by the sputtering method, although the titanium-nitride film (TiN) 16 was shown by the reactive-sputtering method in the inside of the titanium film (Ti) 14 and nitrogen atmosphere and the titanium-nitride film (TiN) 20 was shown by the reactive-sputtering method in the inside of nitrogen atmosphere as 2nd barrier film, it is not limited to a titanium nitride that what is necessary is just what prevents copper oxidization. As the quality of the materials other than this, you may be a silicon nitride, an acid silicon nitride, a titanium nitride, a nitriding tungsten, a titanium-nitride tungsten, a tungsten, chromium, niobium, niobium nitride, aluminum, a tantalum, and a tantalum nitride, for example.
[0083]
[Effect of the Invention] Since the thickness of a wiring layer can be thinly formed according to the manufacture method of the semiconductor device concerning a claim 1 while being able to prevent oxidization of the copper by ashing, in case a sensitization agent is removed as explained above, the embedding property of a between [wiring of a protective coat] is not spoiled, but generating of a void etc. is suppressed, and it becomes possible to take the large margin of the etching conditions of a wiring layer. moreover -- since thickness of a protective coat required for embedding can be made thin -- connection -- the depth of a hole becomes shallow, the time which etching takes becomes short, and a

throughput is improved -- it can make -- connection -- the size controllability of a hole becomes good Furthermore, since the thickness of a wiring layer decreases, a level difference becomes small absolutely and the large margin of the exposure conditions of the upper wiring can be taken. thus, low resistance -- high -- reliable copper wiring can be formed

[0084] the effect according to claim 1 which described above according to the manufacture method of the semiconductor device concerning a claim 2 -- in addition -- since the film of a wiring layer can make much more thin, the embedding property of a wrap protective coat is good in a wiring layer -- becoming -- the thickness of a protective coat -- thin -- it can carry out -- connection -- the depth of a hole becomes shallow, the time which etching takes becomes short, and a throughput improves -- it can make -- connection -- the size controllability of a hole becomes good Moreover, if the thickness of a wiring layer is reduced, a level difference becomes still smaller absolutely and the still larger margin of the exposure conditions of the upper wiring can be taken. thus, low resistance -- high -- reliable copper wiring can be formed

[0085] Since the 1st barrier film and the 2nd barrier film are formed of the quality of the material which prevents oxidization of copper wiring according to the manufacture method of a semiconductor device according to claim 3, oxidization of copper wiring can be certainly prevented with these barrier films.

[0086] According to the manufacture method of a semiconductor device according to claim 4, the film which forms an etching mask Since it consists of the quality of the materials which constitute the so-called hard surface mask blank, ashing at the time of removing an etching mask becomes unnecessary. It can prevent that a copper film oxidizes at the time of ashing, and at the time of etching at the time of forming an etching mask, it can consider as the quality of the material which etch selectivity tends to take between the 2nd barrier film, and an etching mask can be formed certainly.

[0087] Since the film for etching mask formation and the 2nd barrier film were formed with a different membrane type according to the manufacture method of a semiconductor device according to claim 5, in case the film for etching mask formation is **********ed and an etching mask is formed, it becomes possible to take etch selectivity, and an etching mask can be formed certainly.

[0088] Since according to the manufacture method of a semiconductor device according to claim 6 the film for etching mask formation is **********ed and an etching mask is formed so that it may leave the 2nd barrier film, it can avoid oxidizing a copper film, even if ashing removes a sensitization agent.

[0089] Since according to the manufacture method of a semiconductor device according to claim 7 the etching gas containing the compound expressed with CnHmF (2n+2-m) is used in case the film for etching mask formation is **********ed, patterning of the film for etching mask formation can be carried out certainly, and an etching mask can be formed.

[0090] Since the etch rate of the 2nd barrier film was made later than the speed which **********s the film for etching mask formation as etching conditions according to the manufacture method of a semiconductor device according to claim 8, it can leave the 2nd barrier film, patterning of the film for etching mask formation can be carried out certainly, and an etching mask can be formed.

[0091] According to the manufacture method of a semiconductor device according to claim 9, since the gas containing chlorine was used, the etching gas used at the process which forms a wiring layer can prevent oxidization of copper wiring, and can have high-reliability copper wiring by low resistance, without affecting the embedding property of the layer mesenteriolum further.

[0092] Since it was made to ********** using the etching gas by which the compound expressed with CnHmF (2n+2-m) was contained in the process which removes an etching mask according to the manufacture method of a semiconductor device according to claim 10, it can leave the 2nd barrier film and an etching mask can be removed certainly.

[0093] Since it was made to ********** in the process which removes an etching mask and the 2nd barrier film using the etching gas by which 6 sulfur fluoride (CF6) is contained according to the manufacture method of a semiconductor device according to claim 11, it becomes possible to remove an etching mask and the 2nd barrier film certainly.

[0094] According to the manufacture method of a semiconductor device according to claim 12, as etching conditions, since the etch rate of the 2nd barrier film was made later than the etch rate of an

etching mask, it leaves the 2nd barrier film, and it **********s certainly and only an etching mask can be removed.
[0095] According to the manufacture method of a semiconductor device according to claim 13, as etching conditions, since the etch rate of the film for etching mask formation and the etch rate of the 2nd barrier film were made almost equal, an etching mask and the 2nd barrier film are certainly removable.
[0096] According to the manufacture method of a semiconductor device according to claim 14, since the wiring layer front face was processed in gas atmosphere, the layer of a copper wiring layer which prevents oxidization and diffusion on a side attachment wall at least can be formed.
[0097] According to the manufacture method of a semiconductor device according to claim 15, since it was made to carry out solution processing of the wiring layer front face, the layer of a copper wiring layer which prevents oxidization and diffusion on a side attachment wall at least can be formed.
[0098] According to the manufacture method of a semiconductor device according to claim 16, since it was made to pour in an impurity into a wiring layer, the layer of a copper wiring layer which prevents oxidization and diffusion on a side attachment wall at least can be formed.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Conventionally, integrated circuits, such as IC and LSI which formed many elements and wiring with high density on the semiconductor substrate, or a VLSI, are manufactured. In this kind of semiconductor device, in order to realize the further improvement in the speed and the further large-capacity-izing, the degree of integration needed to be raised. However, since reduction of the wiring width of face accompanying this high integration leads to high resistance-ization, it is desirable to use what has resistance small as much as possible as a wiring material. For this reason, recently, it replaces with aluminum etc. and the semiconductor device using the copper which is low electrical resistance materials as a wiring material is proposed.

[0003] Then, a part of manufacturing process of the conventional semiconductor device at the time of using copper as a wiring material is shown in (a) - (c) of drawing 5 . Here, in order to simplify explanation, the explanation about the formation method of a transistor portion is omitted.

[0004] As shown in drawing 5 (a), in order to separate a transistor portion and a wiring layer, on a silicon substrate 50, an insulator layer 52 is formed by the CVD (Chemical Vaper Deposition : chemical vapor deposition) method. And on the insulator layer 52, the titanium film (Ti) 54 was formed by the sputtering method, the titanium-nitride film (TiN) 56 was formed by the reactive-sputtering method or the RTA (Rapid Thermal Anneal) method on it, and the copper film (Cu) 58 was further formed of the sputtering method or CVD on it.

[0005] As shown in drawing 5 (b), after applying the about 1.0-micrometer photoresist 60 on the copper film (Cu) 58 and forming this in a desired circuit pattern with photolithography technology next, the wiring layer was formed by **********ing by the reactive-ion-etching (RIE) method by making this into an etching mask. As etching gas used in case this reactive ion etching is performed, a silicon tetrachloride (SiCl4), nitrogen (N2), and the argon (Ar) were used, for example. Moreover, the temperature of a silicon substrate 50 was low, and since the etch rate was slow, the vapor pressure of the chloride of the copper generated by etching made it about [300 degrees] C. And after removing a photoresist 60 by the oxygen ashing method, as shown in drawing 5 (c), the insulator layer 62 as layer mesenteriolum which embeds between wiring layers was formed.

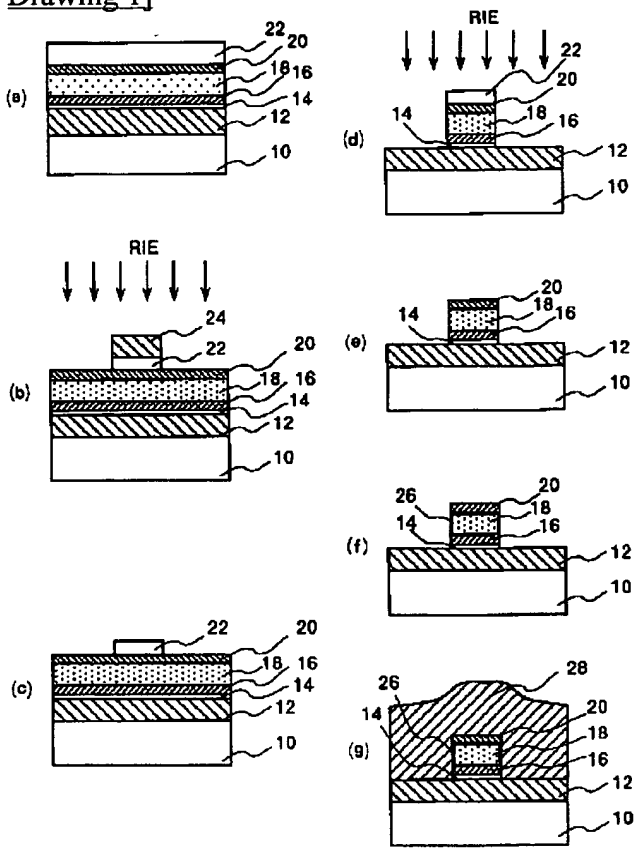
[Translation done.]

DESCRIPTION OF DRAWINGS

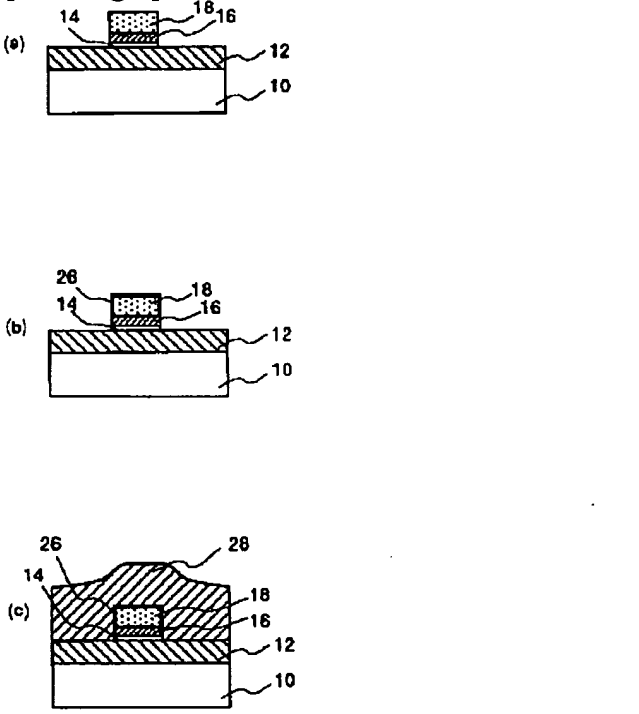
[Brief Description of the Drawings]
[Drawing 1] It is a process cross section explaining the manufacture method of the semiconductor device concerning the gestalt 1 of operation.
[Drawing 2] It is a process cross section explaining the manufacture method of the semiconductor device concerning the gestalt 2 of operation.
[Drawing 3] It is a process cross section explaining the manufacture method of the semiconductor device concerning the gestalt 3 of operation.
[Drawing 4] It is a process cross section explaining the manufacture method of the semiconductor device concerning the gestalt 4 of operation.
[Drawing 5] It is a process cross section explaining the manufacture method of the conventional semiconductor device.
[Description of Notations]
10 Silicon Substrate (Semiconductor Substrate)
12 Insulator Layer
14 Titanium Film (a Part of 1st Barrier Film)
16 Titanium-Nitride Film (a Part of 1st Barrier Film)
18 Copper Film
20 Titanium-Nitride Film (2nd Barrier Film)
22 Silicon Nitride (Film for Etching Mask Formation, Etching Mask)
24 Photoresist (Sensitization Agent)
26 Cu-BTA Compound (Layer Which Prevents Oxidization and Diffusion)
28 Layer Insulation Film (Protective Coat)
30 Copper Silicide (Layer Which Prevents Oxidization and Diffusion)
32 Copper Silicide (Layer Which Prevents Oxidization and Diffusion)

[Translation done.]

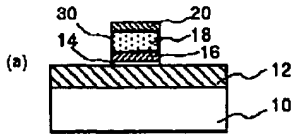
Drawing 1]

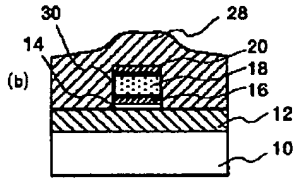


[Drawing 2]

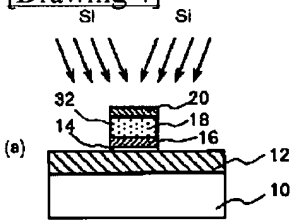


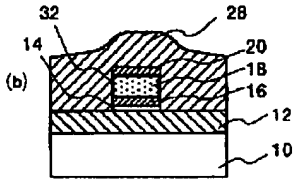
[Drawing 3]



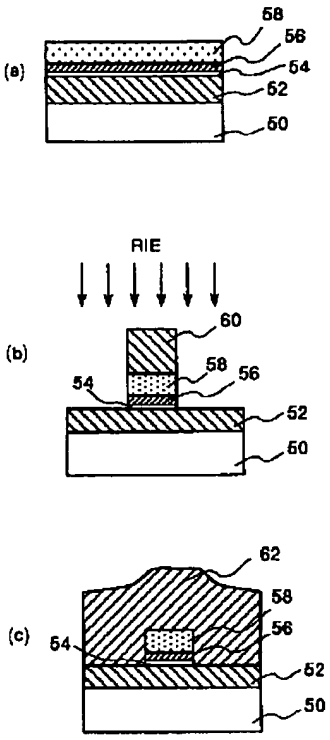


[Drawing 4]





[Drawing 5]



[Translation done.]